

Figure 1

Figure 2A

275

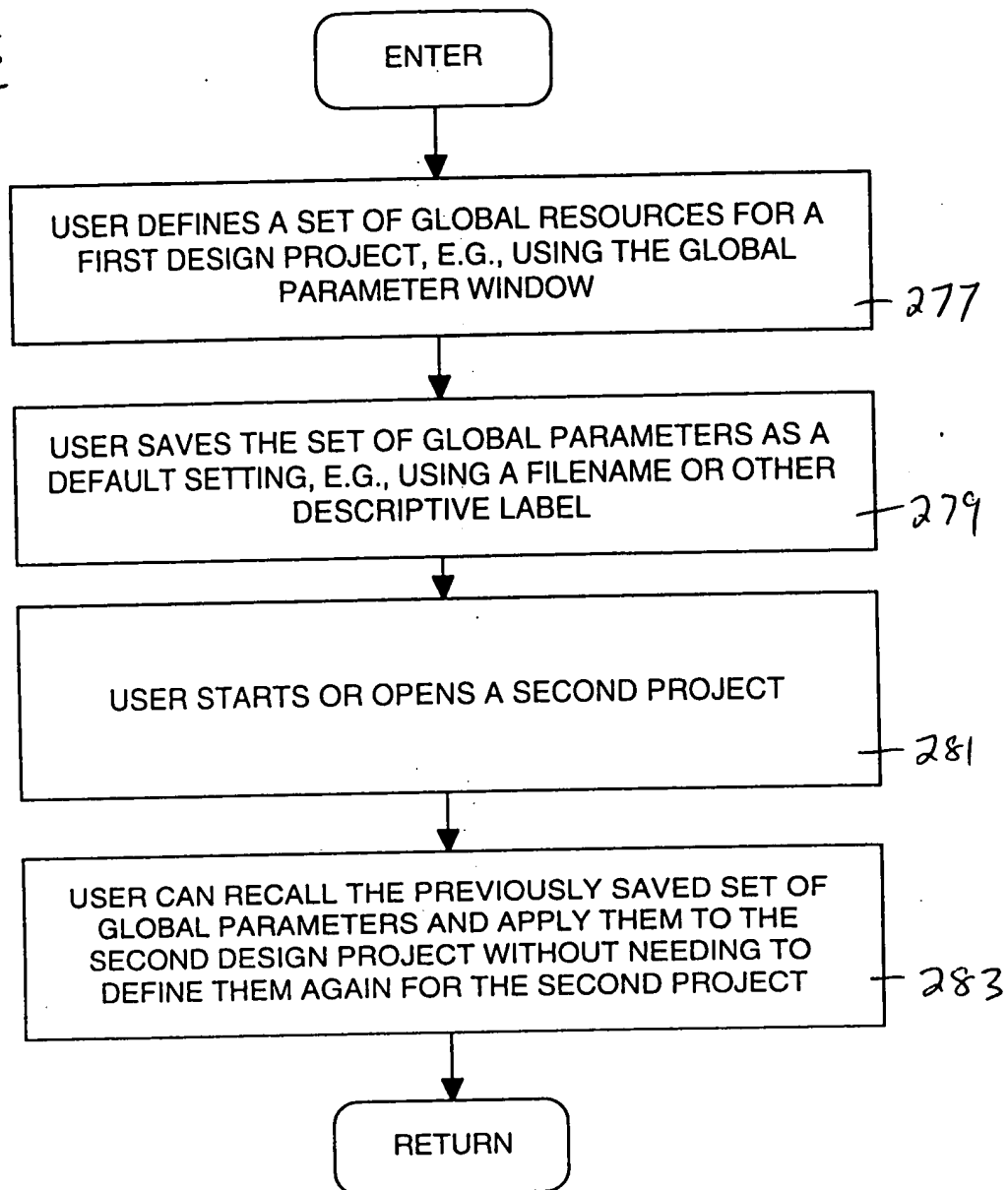


FIG. 2B

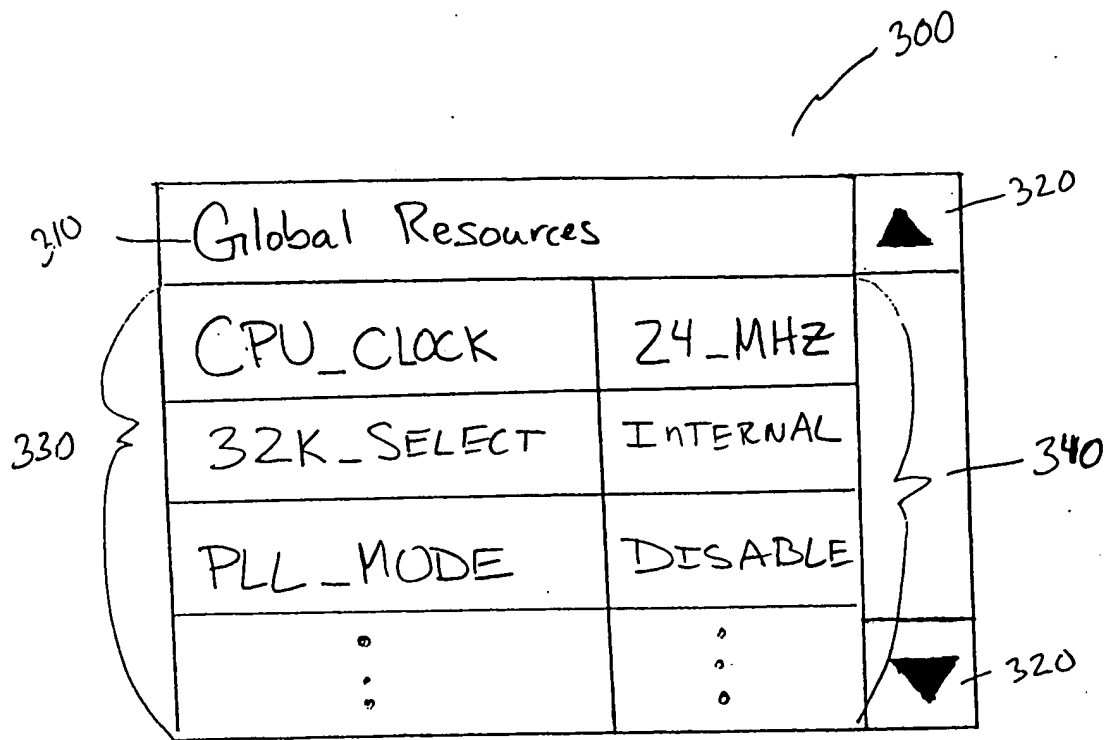


Figure 3

105777 73250550

No. 5505  
Engineer's Computation Pad

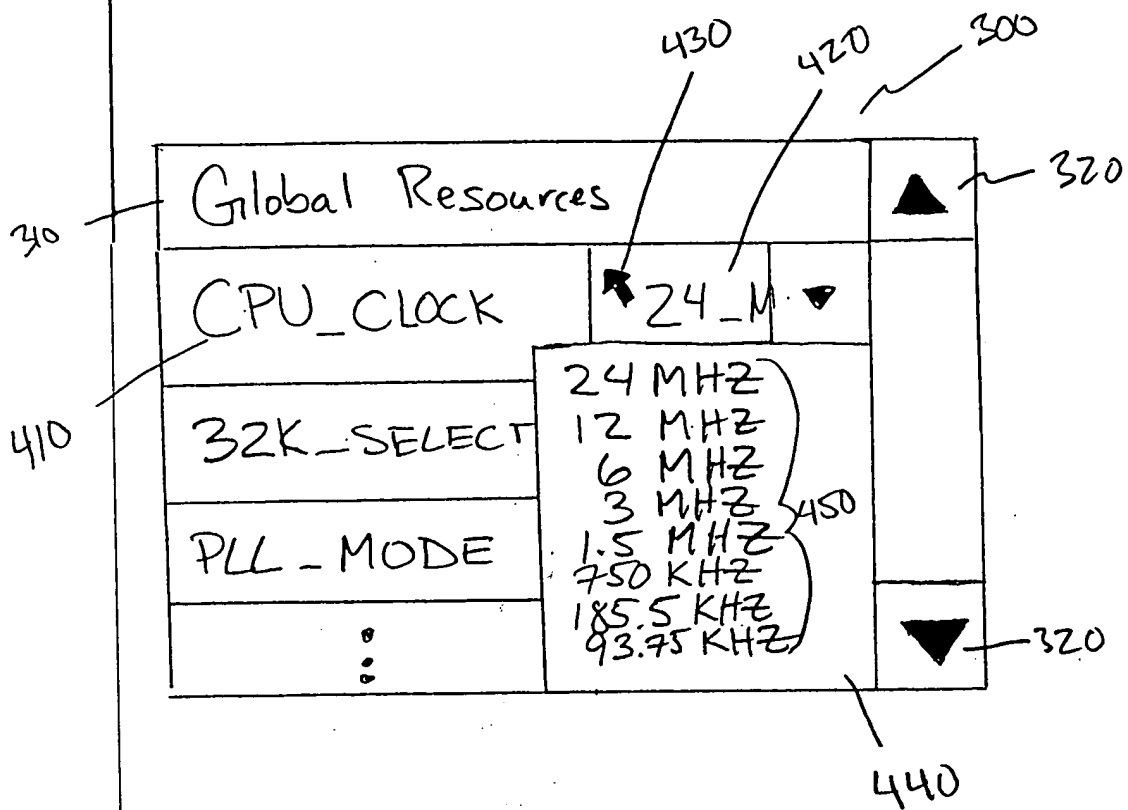


Figure 4

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No. 5505  
Engineer's Computation Pad

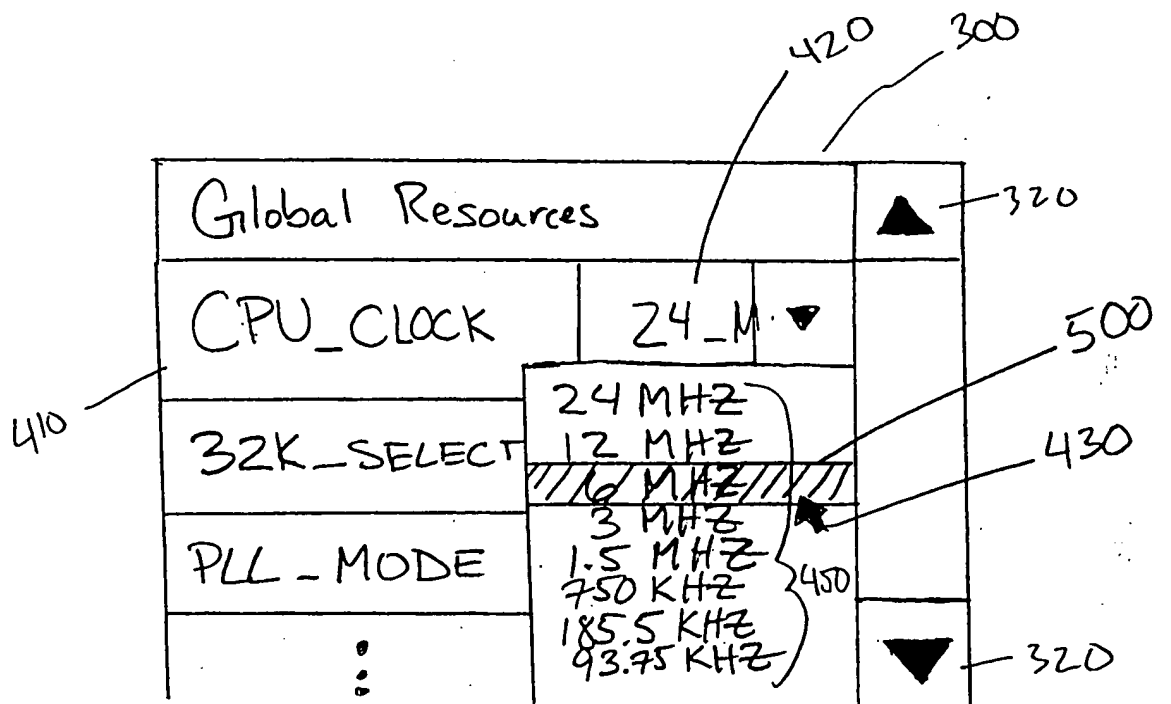
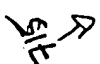


Figure 5





7  
H<sup>is</sup>

0/17



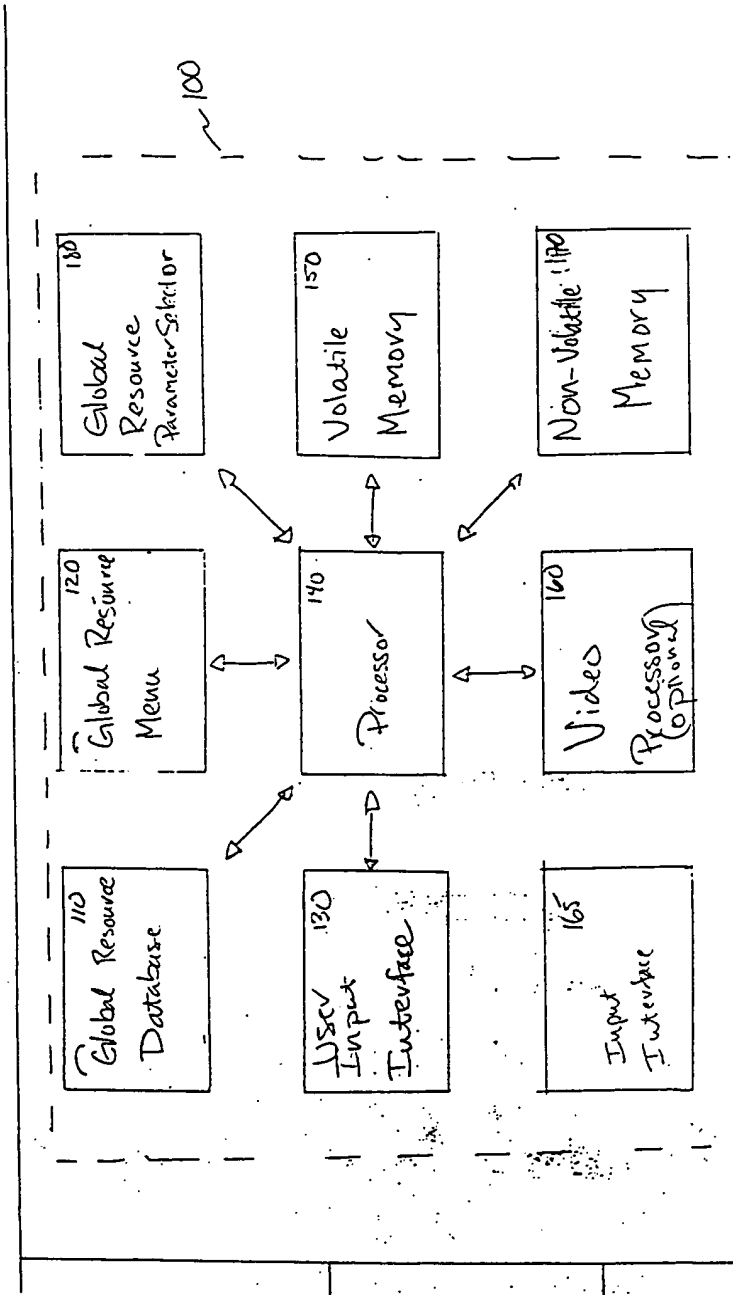


Figure 1

09989761.012803

No. 5505  
Engineer's Computation Pad

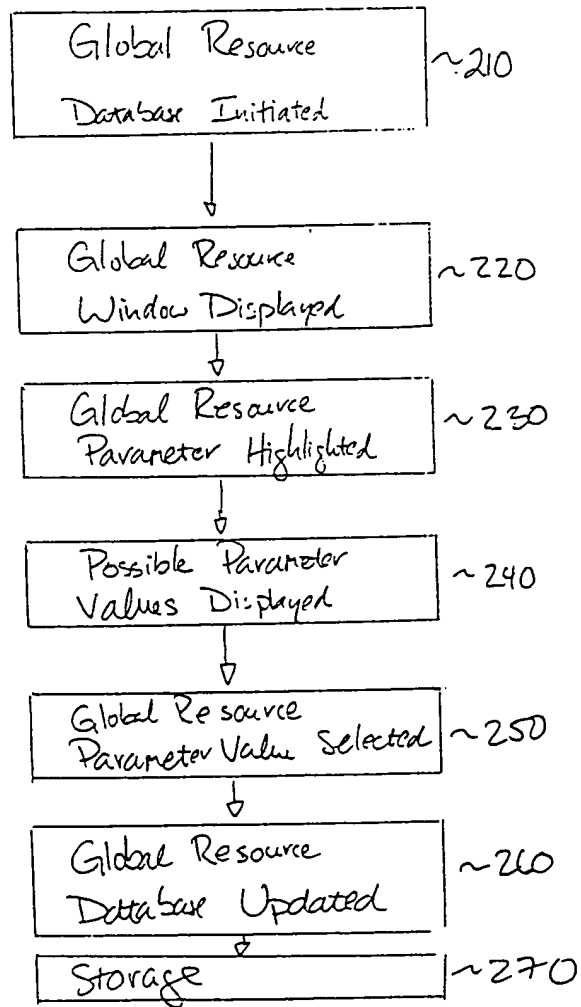


Figure 2A

09989761-012802

275

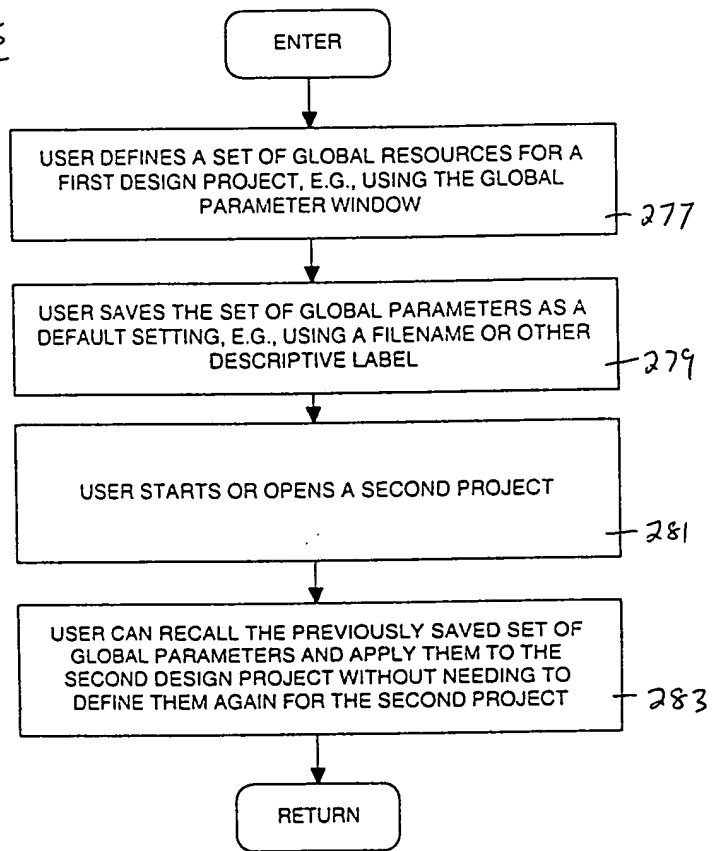


FIG. 2B

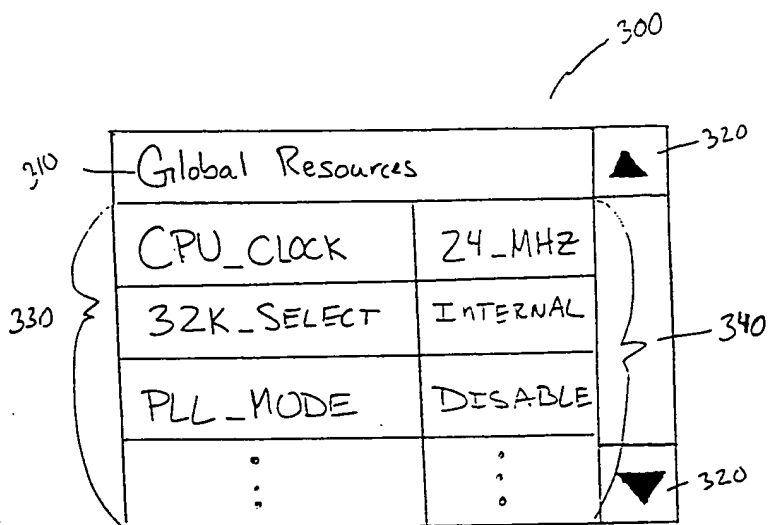


Figure 3

2025.10.10.10.10.10

No. 5505  
Engineer's Computation Pad

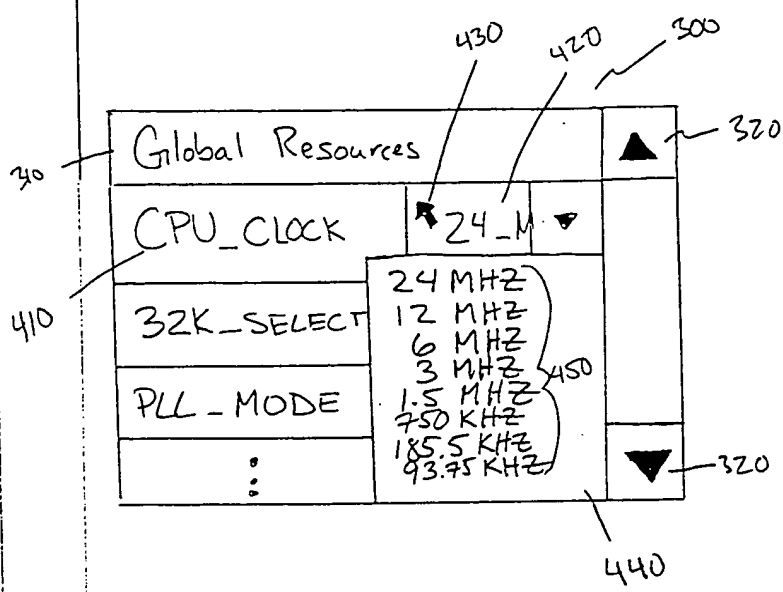


Figure 4

2025-10-10 14:26:50

No. 5505  
Engineer's Computation Pad

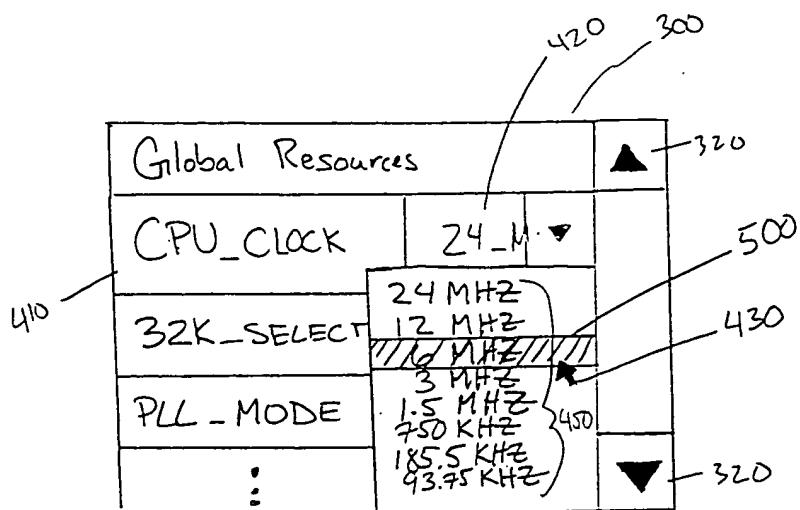
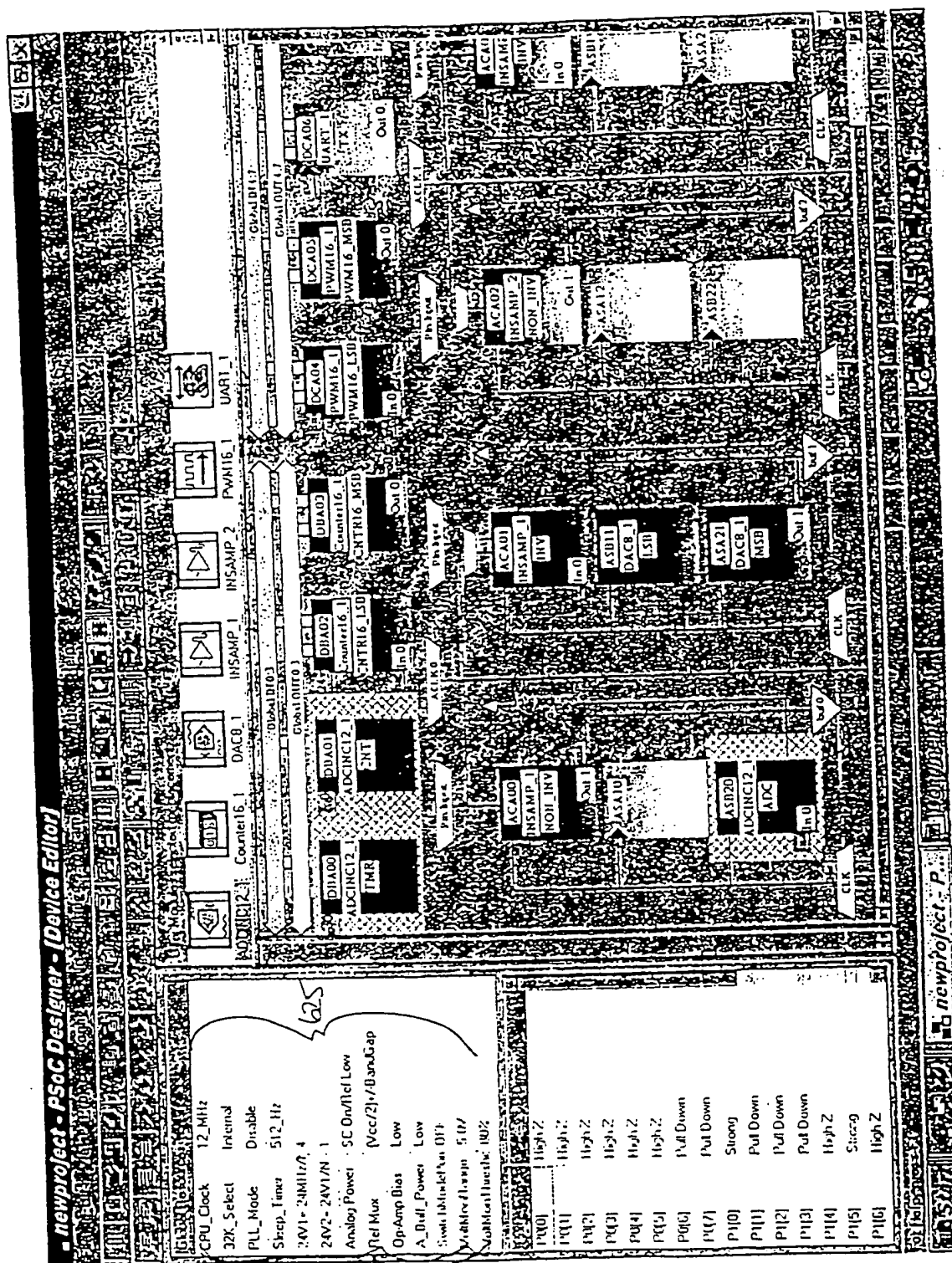


Figure 5

**000000000000**



2  
11

$$\frac{1}{10}$$

**newproject - PSoc Designer - [Device Editor]**

**725**

CPU_Clock	12_MHz
32K_Select	Internal
PLL_Mode	Disable
Sleep_Timer	512_Hz
24V1	24MHz/4
24V2	24V1/N 1
Analog Power	SC On/Rel Low
Ref Mix	Ncc/2)/0-andCap
Up Ave Bias	Ncc/2)/2R-andCap
A_0V1_Power	Ncc/2)/Vcc/2)
SwitchModePw	2 BandGap)/0-andCap
VolModRange	P2(4)/0-andCap
VolMonThresh	P2(4)/P2(5)
	80%

P0[0]	High-Z
P0[1]	High-Z
P0[2]	High-Z
P0[3]	High-Z
P0[4]	High-Z
P0[5]	High-Z
P0[6]	Pull Down
P0[7]	Pull Down
P1[0]	Strong
P1[1]	Pull Down
P1[2]	Pull Down
P1[3]	Pull Down
P1[4]	High-Z
P1[5]	Strong
P1[6]	High-Z

His